REMARKS

Claims 1-20 are pending and all have been rejected under either 35 U.S.C. §§ 102. In response, Applicant is amending claims 1, 9 and 17, canceling claims 7, 8, 15, 16, 19, and 20, and adding claims 21-24. Applicant is also amending the title, submitting a new Abstract, and providing corrections in response to the Examiner's objections. Applicant respectfully submits that all pending and added claims present subject matter that is patentable over the prior art of record, and, in view of the above amendments and following remarks, requests that the Examiner reconsider the application.

SPECIFICATION

In paragraph 3 of the Office Action, the Examiner objected to the Abstract and requested that it be corrected because it exceeded 150 words in length. In response, Applicant is submitting a new Abstract to replace the prior submitted Abstract. The new Abstract includes less than 150 words.

In paragraph 4, the Examiner required that the title be changed because it was not descriptive. The Examiner also suggested a new title. Applicant thanks the Examiner for the suggestion, however, submits the new title as above without referring to "not affecting the architectural state" because that feature is only part of an embodiment of the invention.

CLAIM OBJECTIONS

In paragraph 5a, the Examiner objected to claims 1, 7, 8, 9, 17, 19, and 20 because of informalities. The Examiner indicated that "[c]laims 1, 9, and 17 refer to 'processing' instructions and stopping the 'processing' of instructions in the various stages. However, it is understood from the drawings and description of the operation

of the invention that the 'issuing' of instructions will stop when the instruction queue is full and not the 'execution and retirement' of the instructions. Hence, "processing" leads to some confusion and it is suggested that it be replaced preferably by 'issuing' for purpose of clarity."

Applicant respectfully submit that, in accordance with the third embodiment as described in the Specification, the instructions are processed through various units 130, 140, and 150, etc., and up to a point where the instruction queue 150 is full, at which time *the system* executing the program is frozen or, alternatively, *all units stop processing* instructions (Specification, page 13, lines 18-21). Therefore, Applicant submits that the term *after processing the instructions until the instruction queue is full, stopping processing the instructions in the various stages* is clearly supported by the operation of an embodiment of the invention, and, as a result, Applicant wishes to maintain the term 'processing' in the claims being objected to.

In paragraph 5b, the Examiner objected to claims 7, 8, 19, and 20 because the word "of" should be inserted in between the words "processing the." Applicant is incorporating the features in claims 7, 8, 19, and 20 in their corresponding independent claims, and is therefore canceling those claims. As a result, the objection to those claims is moot.

REJECTIONS UNDER 35 U.S.C. § 102(e) – Sheaffer

In paragraphs 6 and 7, the Examiner rejected claims 1-20 under 35 U.S.C. § 102 (e) as being anticipated by US patent number 006539471B2 to Sheaffer (herein referred to as *Sheaffer*).

Regarding claim 1, the Examiner, in paragraphs 8 and 9, asserted that *Sheaffer* discloses the claimed method.

Applicant is amending claim 1, which currently recites:

A method for retiring instructions . . . , comprising the steps of:
after processing the instructions until the instruction queue is full;,
performing the following steps
stopping processing the instructions in the various processing stages; and
for each instruction in the instruction queue, if the instruction meets the criteria for early retirement, then
terminating the instruction; and
updating a system processing the instruction to reflect that the instruction has been terminated;
wherein the criteria for early retirement is met when at least one of the following conditions is met: continued processing of the instruction does not change the architectural state of the system processing the instruction; continued processing of the instruction has no effect on the behavior of a program running the instruction; the instruction has completed its functions without completing its full pipeline.

Applicant respectfully submits that claim 1 is patentably distinguished from *Sheaffer* for at least several reasons. The claimed invention is about retirement of instructions that meet the early-retirement criteria. Those instructions, as explained in the Specification, do not have any effect on the program behavior after some stages of the pipeline, but continue to use system resources and block launching of subsequent instructions. The existence of these instructions after they have no effect on the overall state of the computation in progress can degrade system performance (page 1, lines 5-15). As claimed in claim 1, the method includes processing instructions until the instruction queue is full. After such time, the method stops processing the instructions and retires instructions that meet the early-retirement criteria, i.e., when one or a combination of the following conditions is met: continued processing of an instruction does not change the architectural state of the system processing the instruction; continued processing of the instruction has no effect on the behavior of a program running the instruction; the instruction has completed its function without completing its full pipeline.

However, none of the paragraphs in *Sheaffer* cited by the Examiner discloses, suggests, or makes obvious the claimed invention. The cited paragraph in col. 1, lines 48-50 discusses that the Re-order buffer (ROB) retires the executed instructions by committing the result(s) to the architectural registers. The cited paragraph in col. 5, lines 21-24 discusses providing the ROB with instructions that have been prepared to be executed. The cited paragraph in col. 5, lines 46-49 discusses that an instruction can be retired when its stop bit is set.

As can be seen, the cited paragraphs do not teach that *after the instruction queue is full*, the instructions that meet the early retirement criteria are terminated. The Examiner admitted that *Sheaffer* does not explicitly teach that "[the] instructions are processed until the ROB is full." Applicant submits further that, in the cited paragraphs, *Sheaffer* does not teach the early-retirement criteria, and therefore cannot logically teach that the instructions that meet the early-retirement criteria are terminated after the instruction queue is full.

The cited paragraphs do not teach that *the retirement criteria is met when at least one of the following conditions is met*: continued processing of an instruction does not change the system architectural state of the system processing the instruction; continued processing of the instruction has no effect on the behavior of a program running the instruction; the instruction has completed its function without completing its full pipeline. Even though *Sheaffer*'s col. 5, lines 45-48 discusses that "if its stop bit is set to so indicate that the instruction can be retired . . ." this cited paragraph does not disclose the details of the criteria cited in Applicant's claim 1.

Neither do the cited paragraphs teach that the (retired) instruction has completed its function without completing its full pipeline (at the time being accessed for early retirement).

Regarding the feature in claim 7 now in claim 1 that the retirement criteria is met when continued processing of the instruction does not change the architectural state of the system processing the instructions, the Examiner, in paragraphs 20 and 21, cited *Sheaffer*'s col. 5, lines 46-49 and col. 8, lines 20-22. *Sheaffer*'s col. 5, lines 45-49 recite "retirement logic 610 reads the stop bit for each instruction in the ROB 606, and retires the instruction (712) if its stop bit is set to so indicate that the instruction can be retired . . . ." *Sheaffer*'s col. 8, lines 20-22 recite "renaming a register specification in the instruction to write the temporary register rather than the architectural register." Applicant submits that the cited paragraphs do not teach, as the Examiner asserted, "*the instruction for which the stop bit is set* such that they can be retired early *do not write to the architectural registers*" (emphasis added). Rather, *Sheaffer* discloses "for *each instruction in the block that writes any of the architectural registers that would be overwritten by another instruction* in the block, . . ., renaming a register specification . . . *to write the temporary register rather than the architectural register*" (col. 8, lines 15-22, emphasis added), which is patentably distinguished from the Examiner's asseretion. For the sake of argument, even if *Sheaffer* taught that the instructions for which the stop bit is set do not write to the architectural registers, the Examiner failed to show as the Examiner asserted that not writing to the architectural registers means do not change the architectural state of the system. After the instruction queue is full, continued processing of an instruction without writing to the architectural registers, in a lot of situations, can still affect on the architectural state of the system.

Regarding the feature in claim 8 now in claim 1 that the early retirement criteria is met when continued processing of the instruction has no effect on the behavior of the program running the instruction, the Examiner, in paragraphs 22 and 23, asserted that the results written are of instructions making up the program and

hence do not cause the program to behave differently, i.e., change its behavior. Applicant respectfully submits that continued processing of the instructions that write the results affects the program behavior because the program causes the act of writing the results.

Because claim 1 recites limitations patentably distinguished from *Sheaffer*, claim 1 is patentable.

Claims 2-6 depend directly or indirectly from claim 1, and are therefore patentable for at least the same reasons as claim 1. Claims 2-6 are also patentable for their additional limitations.

Claim 9 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1. Claims 10-14 depend directly or indirectly from claim 9 and are therefore patentable for at least the same reasons as claim 9. Claims 10-14 are also patentable for their additional limitations.

Claim 17 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1. Claim 18 depends directly from claim 17 and is therefore patentable for at least the same reasons as claim 17. Claim 18 is also patentable for its additional limitations.

In various paragraphs 10-33, the Examiner discussed reasons for rejecting dependent claims. As discussed above, the dependent claims are patentable for at least the same reasons as the independent claims from which the dependent claims depend. Further, Applicant disagrees to the Examiner's assertions regarding the dependent claims. However, Applicant wishes to reserve the rights to respond in details to those assertions at a later time as appropriate.

ADDED CLAIMS

Applicant is adding claims 21-24, which depends from claim 17. Therefore, claims 21-24 are patentable for at least the same reasons as claim 17. Claims 21-24 are also patentable for their additional limitations. Applicant respectfully submits that limitations in claims 21-24 are supported in the Specification, and therefore no new matter is added.

SUMMARY

In conclusion, Applicant respectfully submits that pending claims 1-6, 9-14, and 17 and 18, and added claims 21-24 clearly present subject matter that is patentable over the prior art of record, and therefore requests that the Examiner withdraw the rejections of the pending claims, consider the added claims, and pass the application to issue. If the Examiner has questions regarding this case, the Examiner is invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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